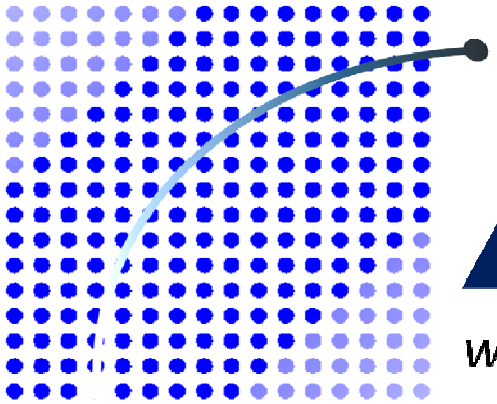
# ADVANPACK SOLUTIONS



APSi

where innovation thrives...

# Technology Licensing & IP Management from APS Perspectives

**Raymond Lim**

**Director (IP & Technology)**

**[Email: sslim@advanpack.com]**

# APS at a Glance

- First incorporated in 1996
- Knowledge-based company since 2005

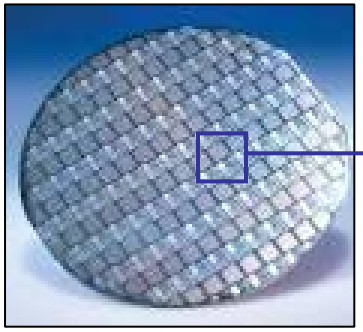
- Industry Field: Semiconductor IC Packaging
- Business Activity: Technology Innovation & Licensing
- IP Protection: Patents, Know-hows

- Products / Technologies Developed:
  - Copper Pillar (CuP)
  - Molded Interconnect Substrate (MIS)
  - Flipchip Packaging

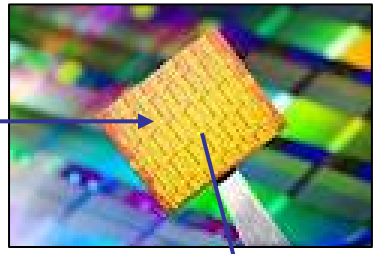
# APS Company Vision

## *"Revolutionize the Semiconductor IC Packaging Industry With APS Innovations"*

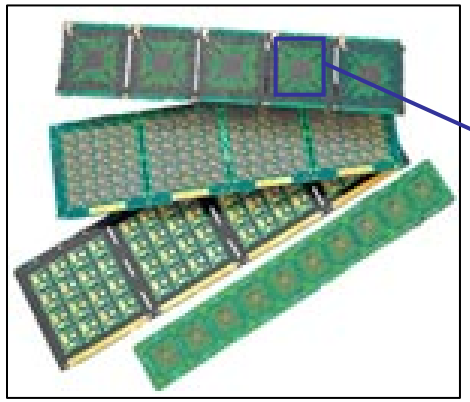
# IC Packaging Overview



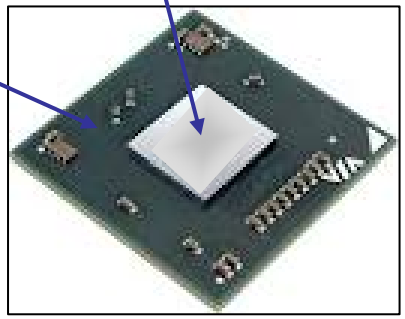
Silicon wafer



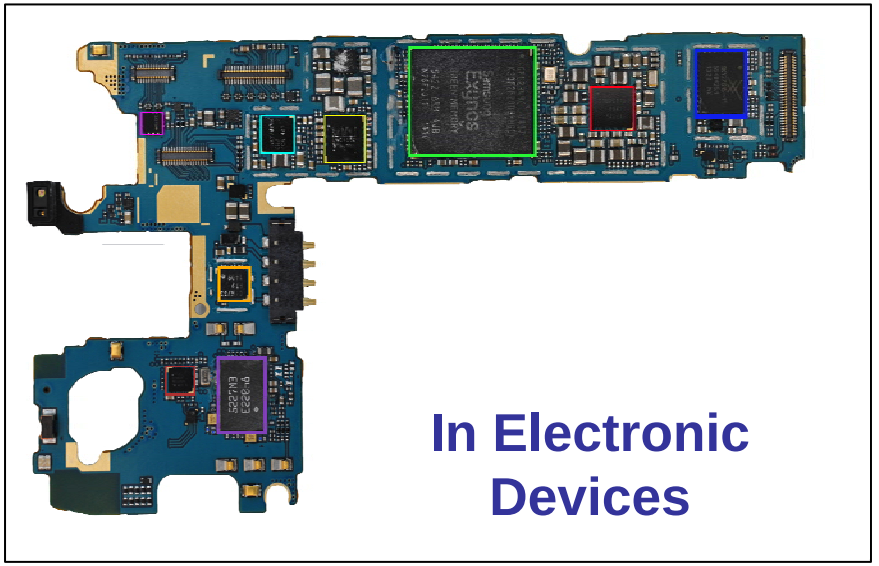
IC chip



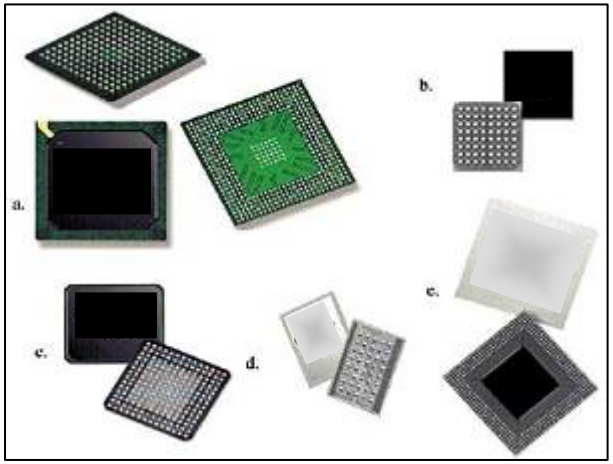
Laminate Substrate



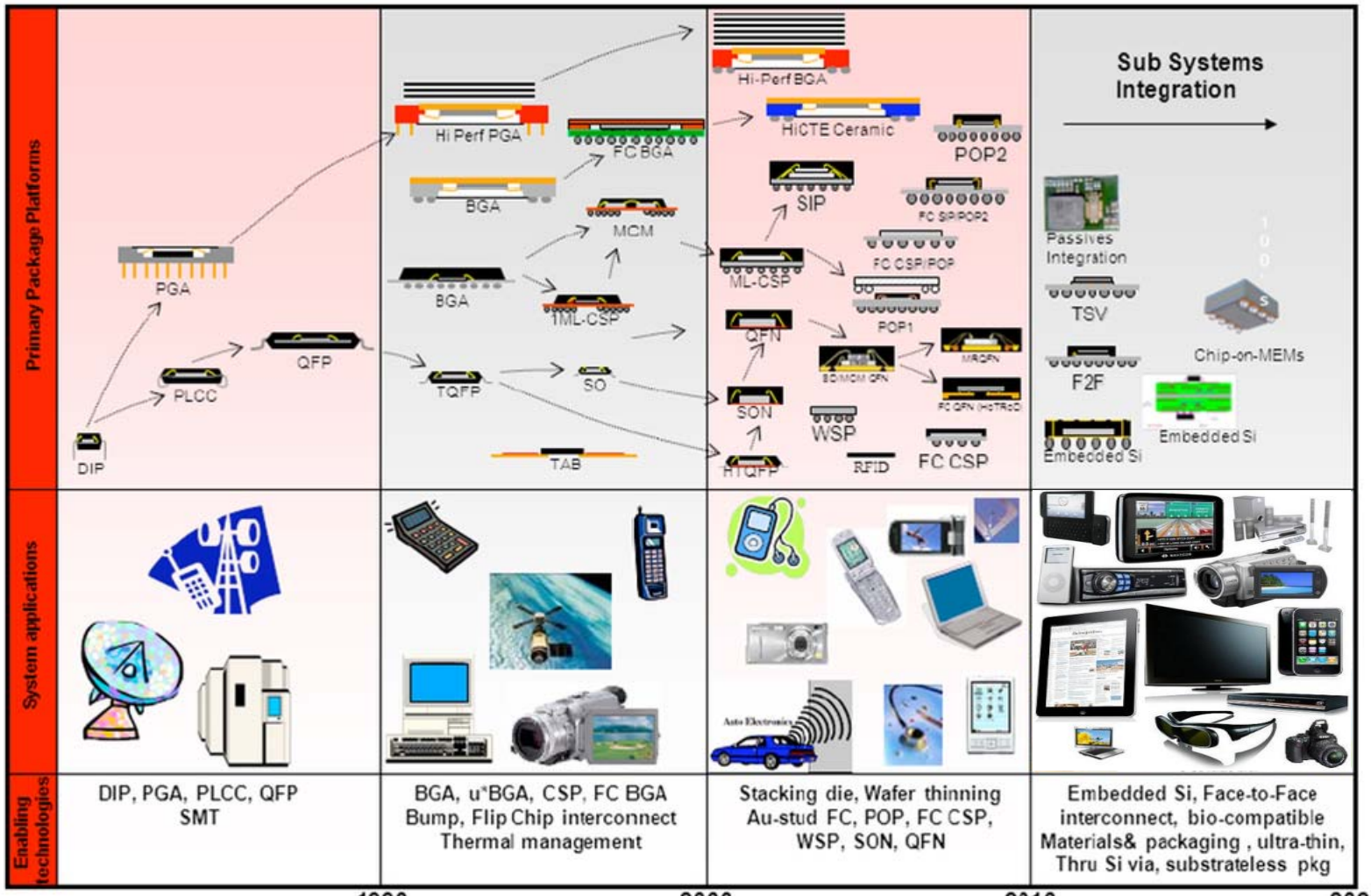
IC Package



In Electronic Devices



# Semiconductor IC Packaging



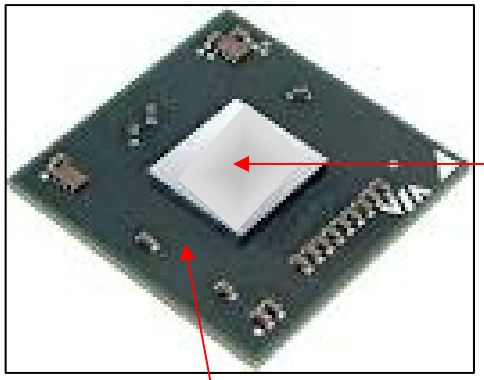

EPTC Dec 7-9, 2011 Keynote talk , MK Iyer, Texas Instruments

©2012 TechSearch International, Inc. at www.techsearchinc.com

Source: Texas Instruments

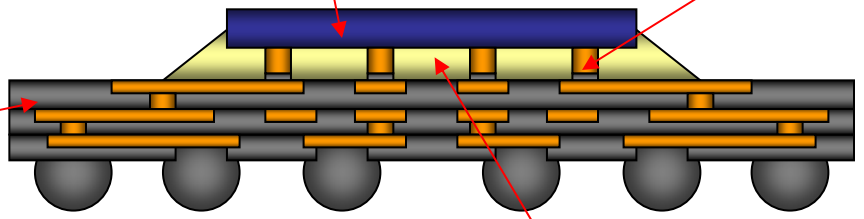
# IC Packaging Overview

IC Package



IC Chip

Electrical Connector



Substrate

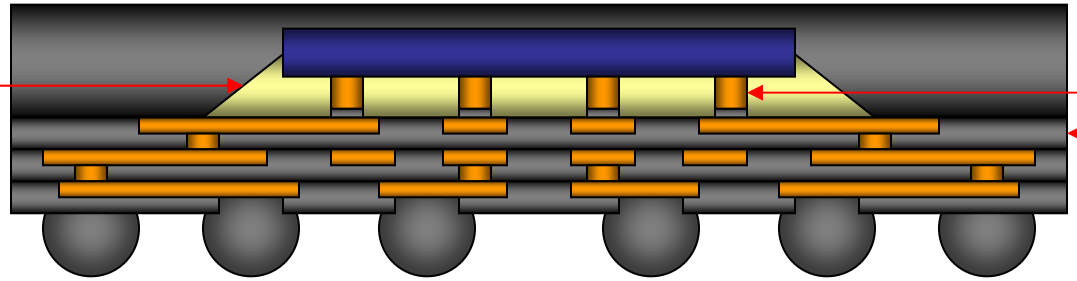
Filling Material

# APS Innovations

## "Revolutionize the Semiconductor IC Packaging Industry with APS Innovations"

**No-Flow Underfill**

**Copper Pillar (CuP)**



**Flipchip Packaging**

**Molded Interconnect Substrate (MIS)**

# Techno IP Centric Business

## APS Functions

- Invention
- Research & Development
- Technology Know-hows
- IP Management
- Business Innovation

→ IP Licensing

→ Technology Transfer

→ Joint Venture

1. Copper Pillar Bump
2. Molded Interconnect Substrate
3. Flipchip Packaging

# Techno IP Centric Business

## "Technology + Intellectual Property"

**Technology Know-hows**

**More than 100 Patent Applications**

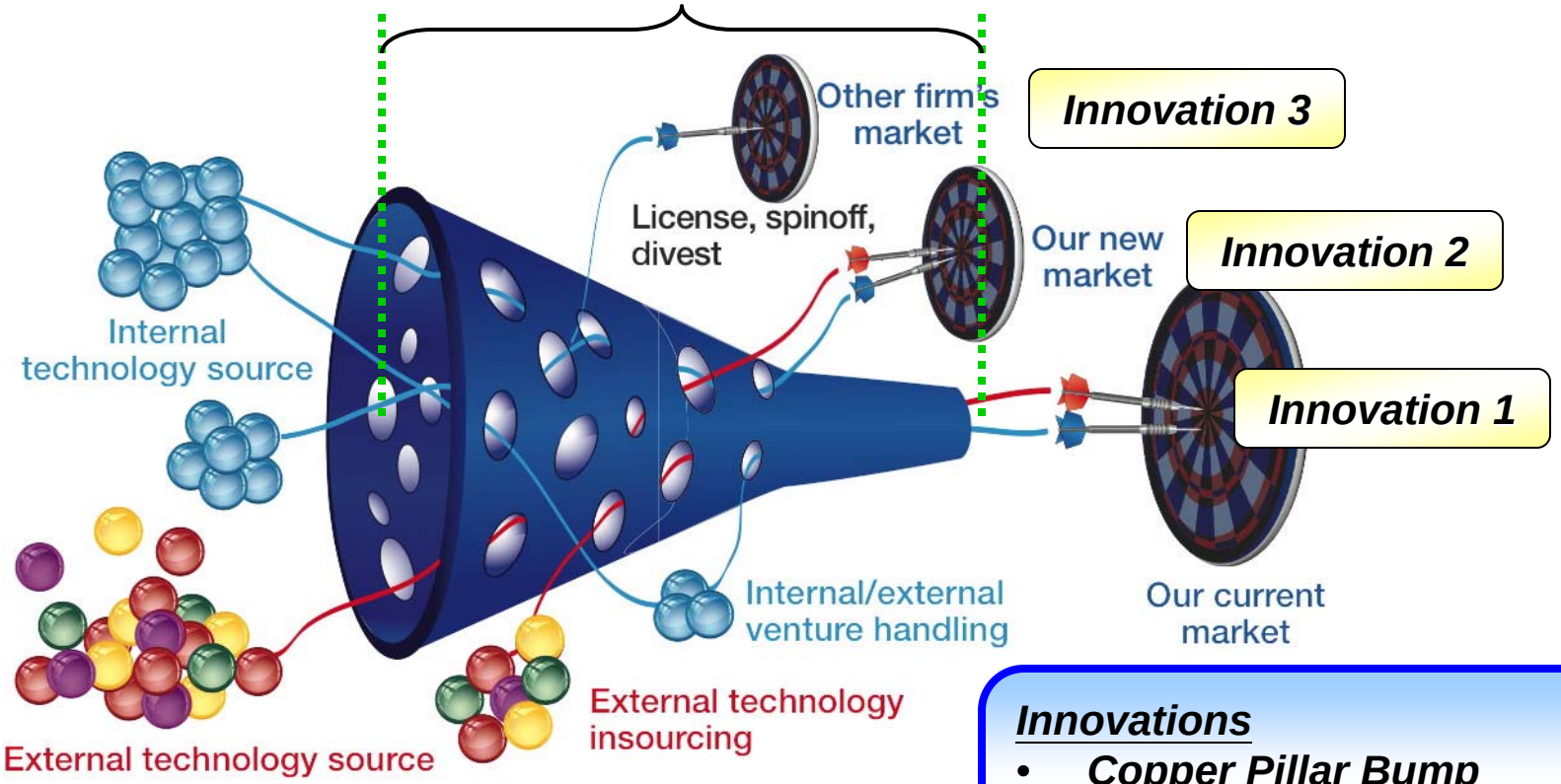
**59 Patents Issued**

**42 Patents Pending**

**As of Dec 2013

# Open Innovation Model

***IP Generation***
***- Patents***
***- Know-hows***




***Innovations***
- ***Copper Pillar Bump***
- ***Molded Interconnect Substrate***
- ***Flipchip Packaging***

***Strategic Partnership***
***- Suppliers / Manufacturers***
***- Research Institutions***

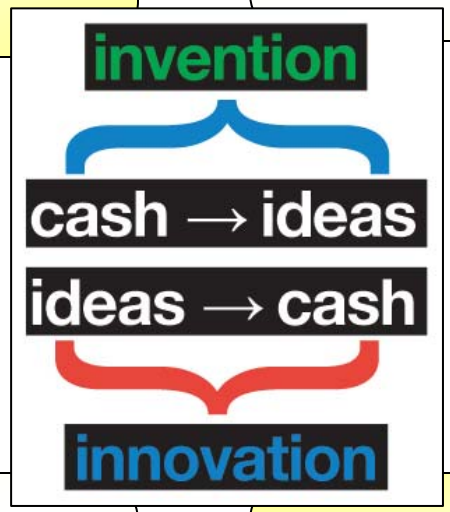
# Funding & Capability Support

### A*STAR GET-UP Initiatives

- T-UP Scheme
- 5 Research engineers Seconded since 2007

### Capability Development Grant

- Support for T-UP secondment fee




Institute of Microelectronics
A*STAR

SPRING singapore
Enabling Enterprise

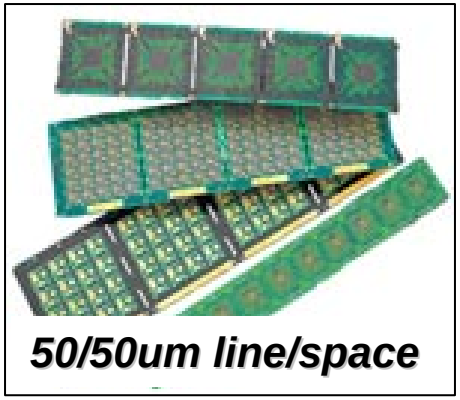
### Research Consortiums

- EPRC 6
- EPRC 11

### Technology Innovation Grant

- Development of MIS technology

# APS Innovations

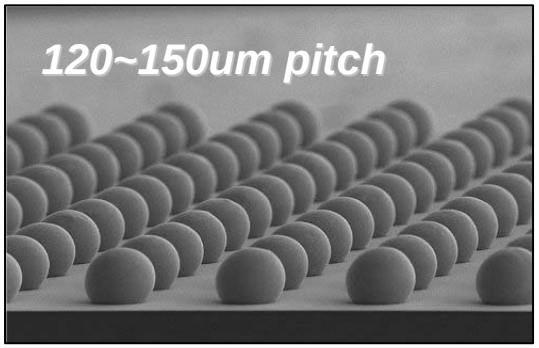


50/50um line/space

Laminate substrate

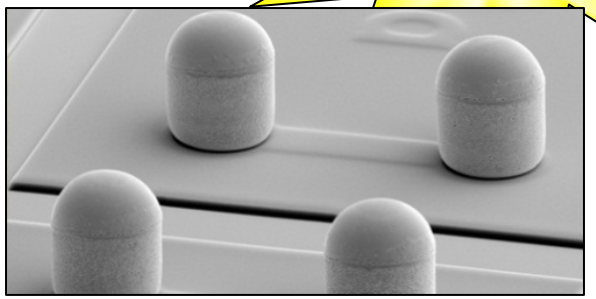
Fine line/space <= 15/15um
Micro-via <= 50um

**Molded Interconnect Substrate (MIS)**




Solder bump

Fine pitch
<= 50um



**Copper Pillar (CuP)**

# APS Patents

## Copper Pillar
## US pat. 6,578,754
## Filed on Apr 27, 2000

US006578754B1

(12) **United States Patent**
**Tung**

(10) **Patent No.: US 6,578,754 B1**
(45) **Date of Patent: Jun. 17, 2003**

(54) **PILLAR CONNECTIONS FOR SEMICONDUCTOR CHIPS AND METHOD OF MANUFACTURE**

(75) Inventor: **Francisca Tung**, Austin, TX (US)

(73) Assignee: **Advanpack Solutions Pte. Ltd.**, Singapore (SG)

( * ) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/564,382**

(22) Filed: **Apr. 27, 2000**

(51) **Int. Cl.**[7] ..... **B23K 35/14**
(52) **U.S. Cl.** ..... **228/180.22**; 228/123.1
(58) **Field of Search** ..... 228/180.22, 254, 228/123.1, 193–195, 56.3; 428/403, 209, 643, 644, 570; 148/24; 106/286.2, 287.19; 438/613–617; 257/737–738

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| | | | |
|---|---|---|---|
| EP | 0602328 | A2 | 9/1993 |
| EP | 0889512 | A2 | 4/1998 |
| JP | 04037139 | | 5/1992 |

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"A fine pitch and high aspect ratio bump fabrication process for flip–chip interconnection," by Yamada et al., Electronic Manuf. Tech. Symp., 1995, Proceedings of 1995 Japan Int'l 18th, IEEE/CPMT Int'l Omiya, Japan, Dec. 4–6, 1995, New York, NY, USA, IEEE, pp. 121–124 XP010195564.

"Wire Interconnect Technology, a New High–Reliability Tight–Pitch Interconnect Technology," D. Love et al., Fijitsu Computer Packaging Technologies, Inc., ITAP (International TAB, Flip Chip and BGA Packaging Conference) Feb. 1996,, 7 pages.

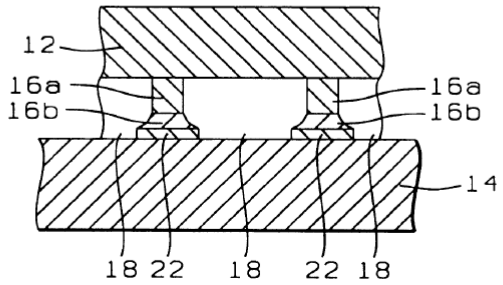
* cited by examiner

*Primary Examiner*—Tom Dunn
*Assistant Examiner*—Jonathan Johnson
(74) *Attorney, Agent, or Firm*—George O. Saile; Stephen B. Ackerman

(57) **ABSTRACT**

A flip chip interconnect system comprises and elongated pillar comprising two elongated portions, one portion including copper and another portion including solder. The portion including copper is in contact with the semiconductor chip and has a length preferably of more than 55 microns to reduce the effect of α particles from the solder from affecting electronic devices on the chip. The total length of the pillar is preferably in the range of 80 to 120 microns.

**9 Claims, 6 Drawing Sheets**




## Molded Interconnect Substrate
## US pat. 7,795,071
## Filed on Sep 14, 2007

US007795071B2

(12) **United States Patent**
**Hwee-Seng Jimmy et al.**

(10) **Patent No.: US 7,795,071 B2**
(45) **Date of Patent: Sep. 14, 2010**

(54) **SEMICONDUCTOR PACKAGE FOR FINE PITCH MINIATURIZATION AND MANUFACTURING METHOD THEREOF**

(75) Inventors: **Chew Hwee-Seng Jimmy**, Singapore (SG); **Ong Chee Kian**, Singapore (SG); **Abd. Razak Bin Chichik**, Singapore (SG)

(73) Assignee: **Advanpack Solutions Pte Ltd.**, Singapore (SG)

( * ) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **11/898,717**

(22) Filed: **Sep. 14, 2007**

(65) **Prior Publication Data**

US 2008/0145967 A1 Jun. 19, 2008

**Related U.S. Application Data**

(63) Continuation-in-part of application No. 11/882,194, filed on Jul. 31, 2007, now abandoned.

(30) **Foreign Application Priority Data**

Dec. 14, 2006 (TW) ..... 95146945 A

(51) **Int. Cl.**
***H01L 21/00*** (2006.01)

(52) **U.S. Cl.** ..... **438/106**; 257/666; 257/667; 257/673; 257/708; 257/710; 257/E23.01; 257/E23.023; 257/E23.031; 257/E23.034; 257/E23.036; 438/111; 438/112

(58) **Field of Classification Search** ..... 438/106, 438/111, 112; 257/666, 673, 676, 667, 668, 257/688, 690–691, 708, 710, 678, E23.01, 257/E23.023, E23.031, E23.034, E23.036, 257/E23.065, E23.06, E23.062, E23.07; 174/261–262; 361/820, 767, 777, 783, 770, 762, 679, 748
See application file for complete search history.

(56) **References Cited**

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| 2003/0194855 | A1 | 10/2003 | Park et al. | |
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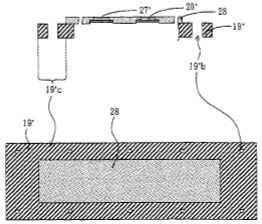
* cited by examiner

*Primary Examiner*—A. Sefer
*Assistant Examiner*—Ermias Woldegeorgis
(74) *Attorney, Agent, or Firm*—Rabin & Berdo, PC

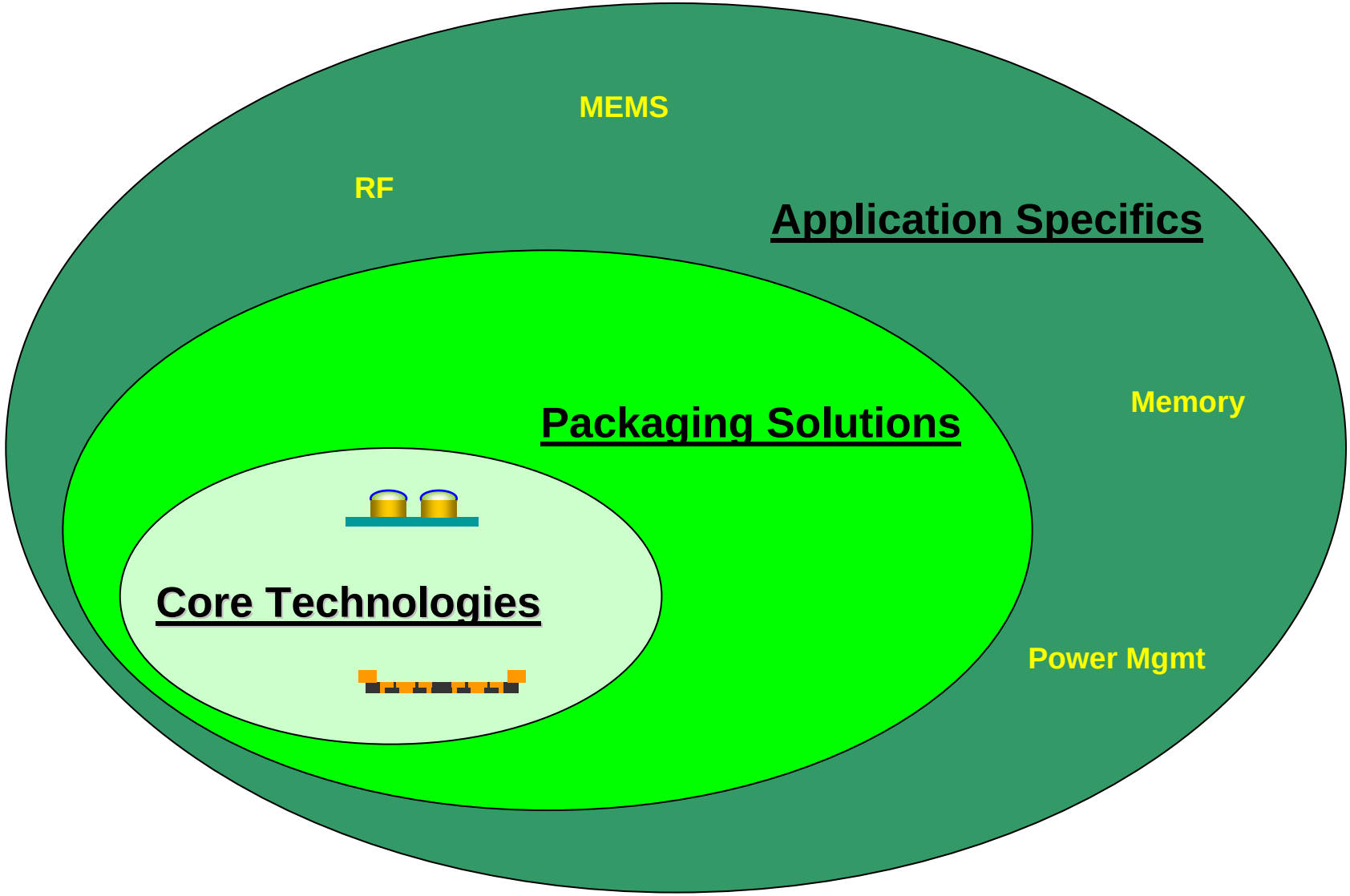
(57) **ABSTRACT**

A semiconductor package and a manufacturing method thereof are provided. The package element has a first insulating layer, and a plurality of holes are disposed on the first surface of the first insulating layer. Besides, a plurality of package traces are embedded in the insulating layer and connected to the other end of the holes. The holes function as a positioning setting for connecting the solder balls to the package traces, such that the signal of the semiconductor chip is connected to the package trace via conductor of the chip, and further transmitted externally via solder ball. The elastic modulus of the material of the first insulating layer is preferably larger than 1.0 GPa.

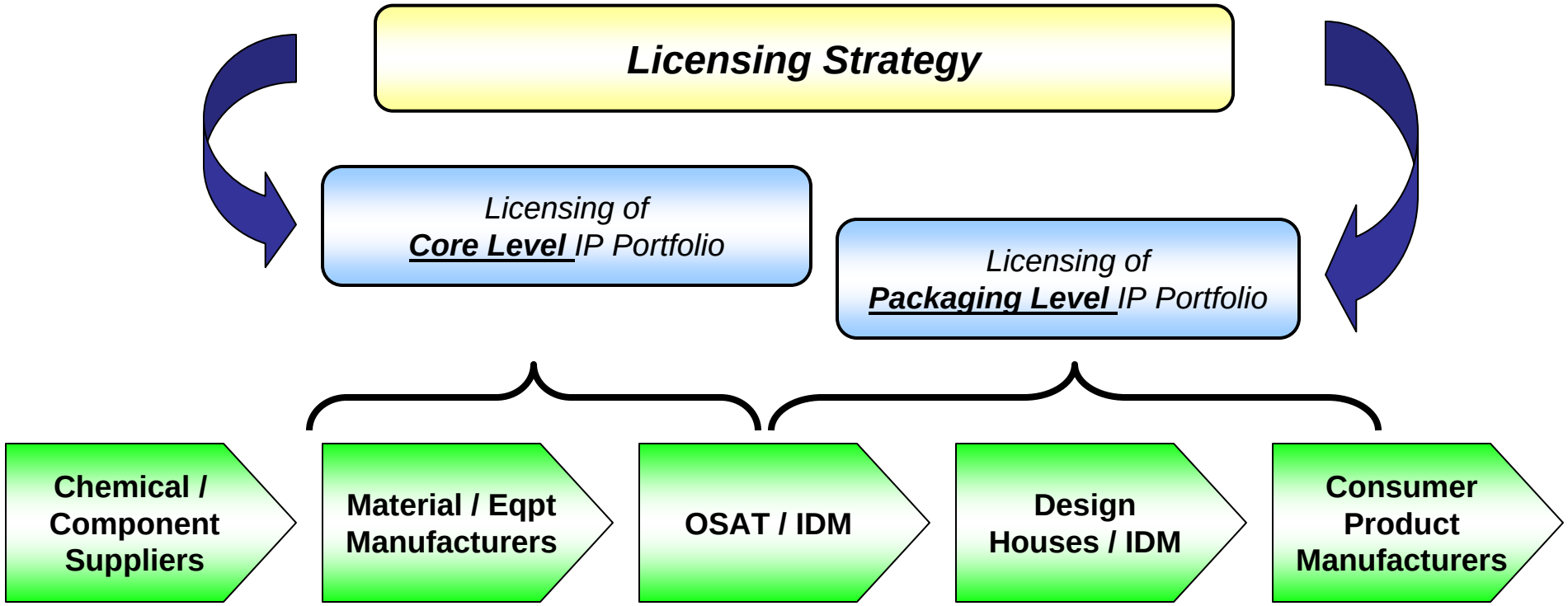
**4 Claims, 11 Drawing Sheets**



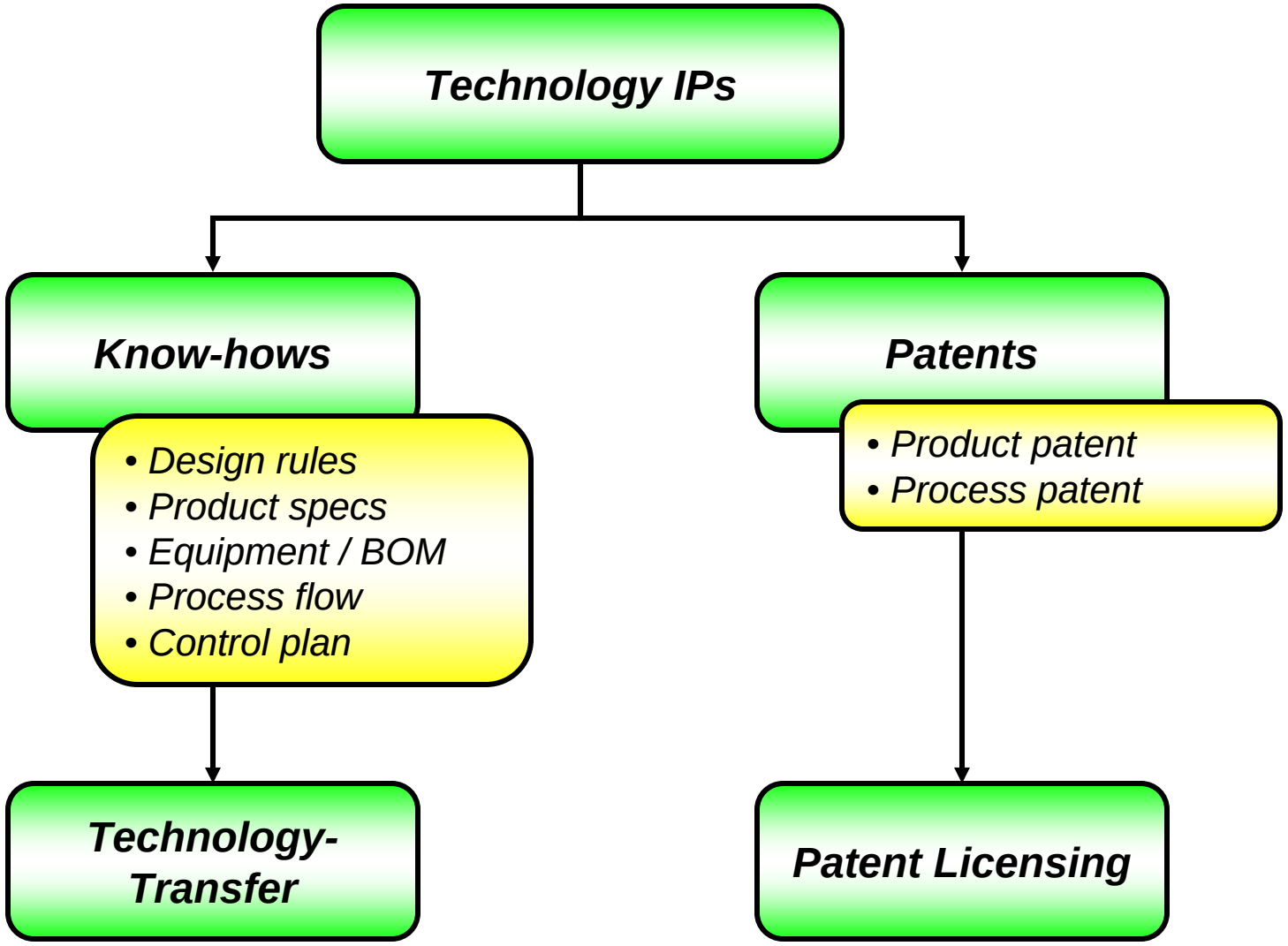
# IP Strategy – Patenting



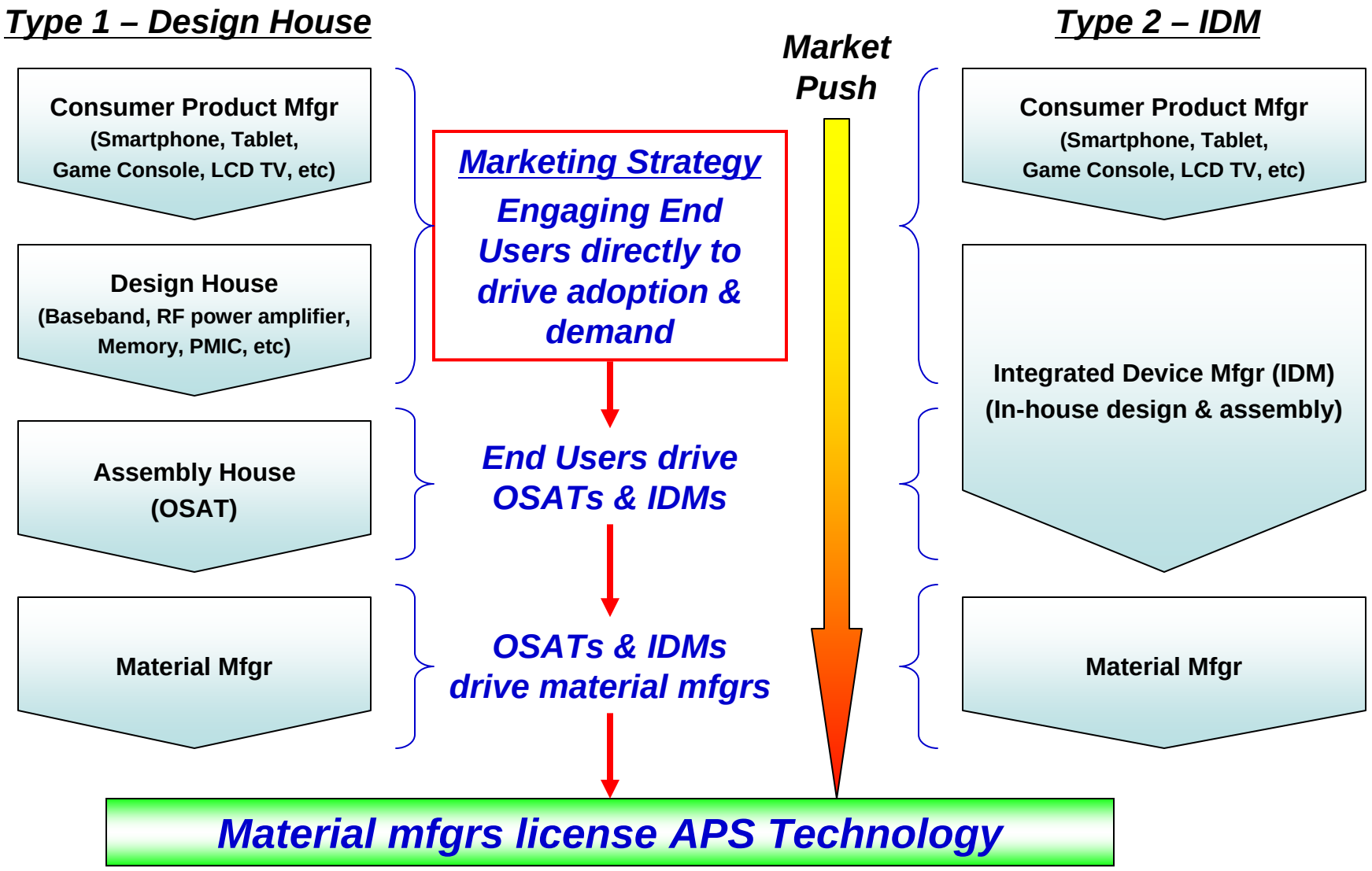
# IP Strategy – Licensing



# IP Strategy – Licensing



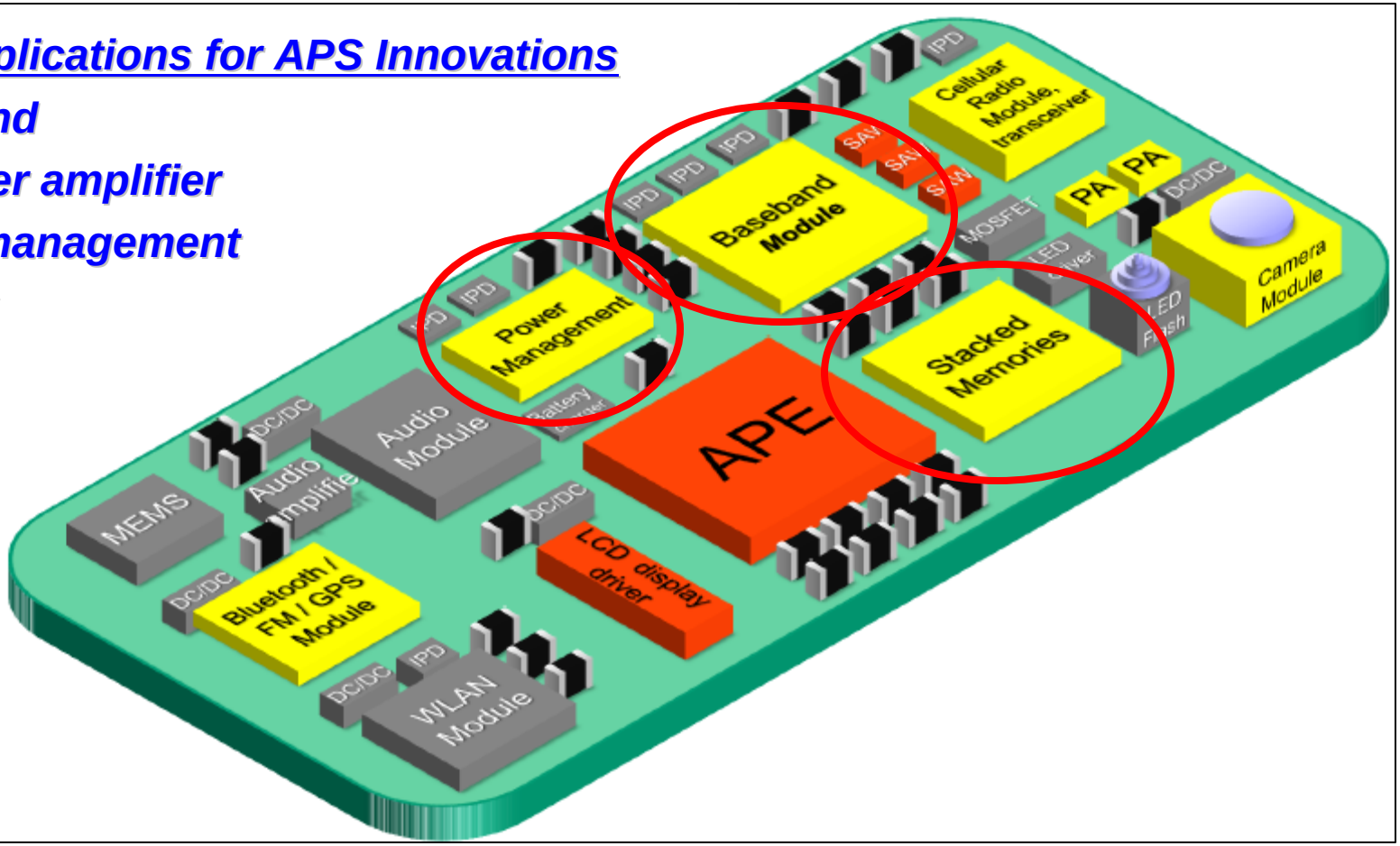
# Commercialization / Marketing Strategy



# Commercialization / Marketing Strategy

## Target Applications for APS Innovations

- Baseband
- RF power amplifier
- Power management
- Memory

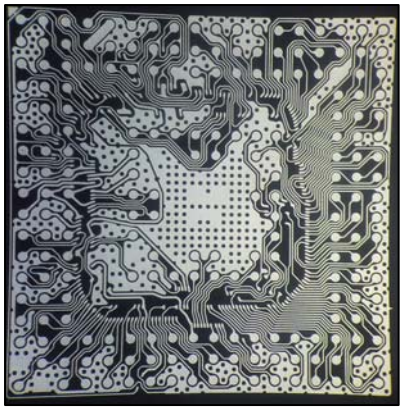


# Commercialization / Marketing Strategy

**Target Customers**


Source: Gartner, Company data, Nomura estimates, * not covered by Nomura

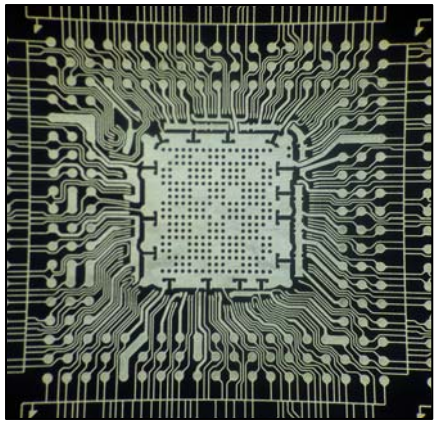
# APS Innovations - MIS Substrate

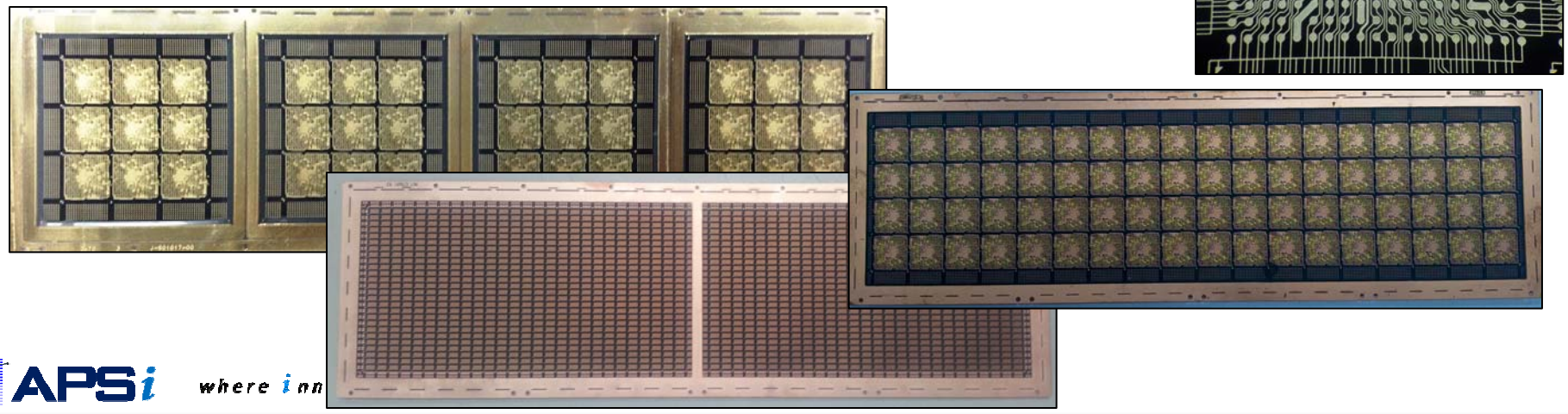


## Key Business Outcome to Date

- ***5 Licensees***
- ***2 Licensees in Pipeline for 2014***

- ***Technology Impact***
  - Revolutionize Semiconductor Substrate Industry
    - Novel manufacturing concept
    - Improve product features
    - Reduce cost by 20~50%



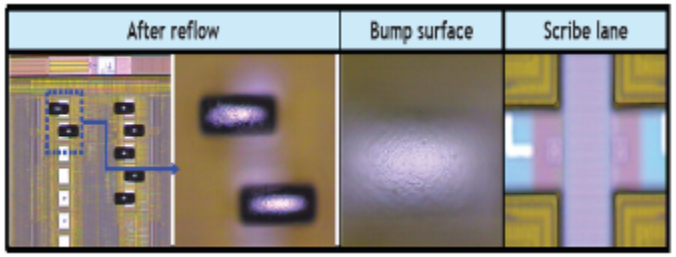


# APS Innovations - CuP Bump

## Key Business Outcome to Date

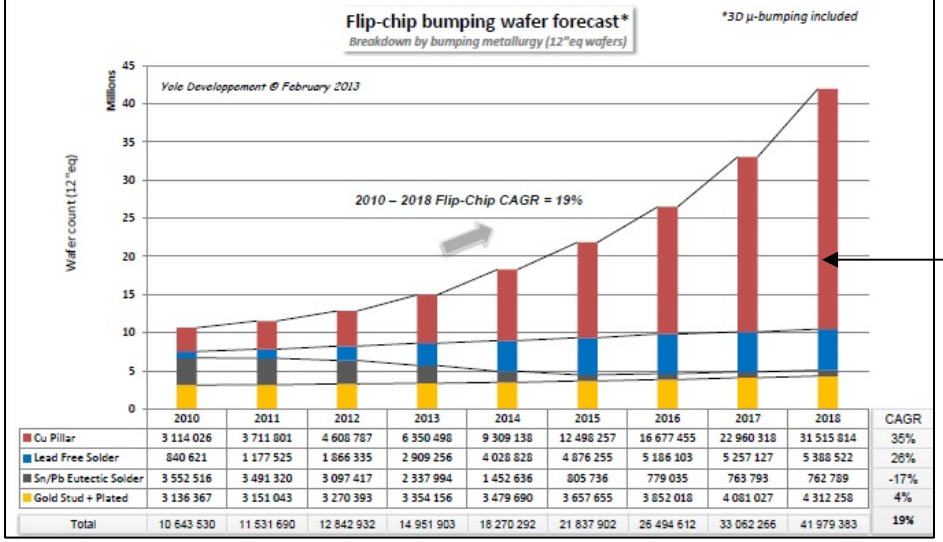
- *2 Joint Ventures*
  - *In China*
  - *In Malaysia*
- *10 Licensees*

*Pillar bump*




*Elongated pillar bump*

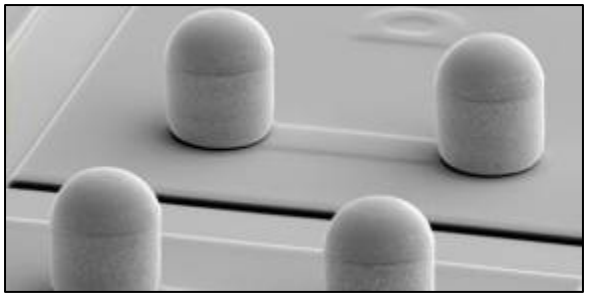
**Flip-Chip wafer forecast by bumping metallurgy**




| | 2010 | 2011 | 2012 | 2013 | 2014 | 2015 | 2016 | 2017 | 2018 | CAGR |
|---|---|---|---|---|---|---|---|---|---|---|
| Cu Pillar | 3 114 026 | 3 711 801 | 4 608 787 | 6 350 498 | 9 309 138 | 12 498 257 | 16 677 455 | 22 960 318 | 31 515 814 | 35% |
| Lead Free Solder | 840 621 | 1 177 525 | 1 866 335 | 2 909 256 | 4 028 828 | 4 876 255 | 5 186 103 | 5 257 127 | 5 388 522 | 26% |
| Sn/Pb Eutectic Solder | 3 552 516 | 3 491 320 | 3 097 417 | 2 337 994 | 1 452 636 | 805 736 | 779 035 | 763 793 | 762 789 | -17% |
| Gold Stud + Plated | 3 136 367 | 3 151 043 | 3 270 393 | 3 354 156 | 3 479 690 | 3 657 655 | 3 852 018 | 4 081 027 | 4 312 258 | 4% |
| Total | 10 643 530 | 11 531 690 | 12 842 932 | 14 951 903 | 18 270 292 | 21 837 902 | 26 494 612 | 33 062 266 | 41 979 383 | 19% |

Source: Yole Development

*Pillar bump wafers*



# Thank You
# for Your Attention